AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (currently amended) A method, comprising:

determining at a requesting agent processor that Input Output (IO) traffic is to be received at a target processor cache, wherein the target processor is different than the requesting agent processor;

receiving from the requesting agent processor routing information associated with the IO traffic; and

arranging for the IO traffic to be transferred directly into the target processor cache in accordance with the routing information, wherein the arranging is performed by at least one of: (i) a direct memory access controller, or (ii) a IO controller hub.

2. (previously presented) The method of claim 1, wherein the routing information is received from an IO driver executing at the requesting agent processor.

3. (previously presented) The method of claim 1, wherein the routing information includes at least one of: (i) a memory address, (ii) a target processor identifier, (iii) a direct transfer on/off indication, (iv) a cache allocation/update indication, (v) a routing policy, (vi) a routing condition, (vii) a routing preference, (viii) coherence information, or (ix) an allocation policy.

4. (previously presented) The method of claim 1, wherein the IO traffic is associated with at least one of: (i) a network, (ii) a network interface controller, (iii) a disk drive controller, (iv) a

peripheral component interconnect interface, (v) a universal serial bus interface, or (vi) a 1394 interface.

5. (original) The method of claim 1, wherein the arranging is performed in a multi-processor system that includes a plurality of potential target processor caches.

6. (canceled)

7. (original) The method of claim 1, wherein the IO traffic includes information packets.

8. (original) The method of claim 1, further comprising:

receiving the IO traffic; and

determining whether the IO traffic should be stored in system memory or be transferred directly into the target processor cache.

9. (original) The method of claim 1, wherein the routing information indicates that one type of IO traffic should be transferred directly into the target processor cache while another type of IO traffic should be transferred directly into another target processor cache.

10. (previously presented) The method of claim 1, wherein the IO traffic is received from at least one of: (i) a network fabric, and (ii) a disk drive, a (iii) a graphics device, or (iv) a peripheral device.

11. (original) The method of claim 1, wherein the IO traffic is transferred into the target processor cache in accordance with a chipset's platform routing function.

12. (currently amended) An article, comprising:

a first storage medium having stored thereon instructions that when executed by a machine result in the following:

determining at a requesting agent processor that Input Output (IO) traffic is to be received at a target processor cache, wherein the target processor is different than the requesting agent processor;

a second storage medium having stored thereon instructions that when executed by a machine result in the following:

receiving from the requesting agent processor routing information associated with the IO traffic; and

arranging for the IO traffic to be transferred directly into the target processor cache in accordance with the routing information, wherein the arranging is performed by at least one of: (i) a direct memory access controller, or (ii) a IO controller hub.

13. (previously presented) The article of claim 12, wherein, wherein the routing information is received from an IO driver executing at the requesting agent processor.

14. (previously presented) The article of claim 12, wherein the routing information includes at least one of: (i) a memory address, (ii) a target processor identifier, (iii) a direct transfer on/off indication, (iv) a cache allocation/update indication, (v) a routing policy, (vi) a

routing condition, (vii) a routing preference, (viii) coherence information, or (ix) an allocation policy.

15-19. (canceled)

20. (currently amended) A system, comprising:

a network fabric;

a network interface controller coupled to the network fabric;

a requesting agent processor;

a target processor having a target cache, wherein the target processor is different than the requesting agent processor; and

a write agent, including:

an input path to receive from the requesting agent processor routing information associated with Input Output (IO) traffic; and

a processing element to arrange for the IO traffic to be transferred directly into a target processor cache in accordance with the routing information, wherein the write agent comprises at least one of: (i) a direct memory access controller, or (ii) a IO controller hub.

21. (original) The system of claim 20, wherein an IO driver executing at the requesting processor provides the routing information to the write agent.

22. (new) A method, comprising:

receiving from a requesting agent routing information associated with Input Output traffic; and

arranging for the IO traffic to be transferred directly into a target processor cache in accordance with the routing information, wherein the arranging is performed by at least one of: (i) a direct memory access controller, or (ii) a IO controller hub.